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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/722,705 | 11/28/2000 | Yoshihiro Yanagisawa | 35.C13918 | 5179 |

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| EXAMINER | |
|---|---|
| RAMSEY, KENNETH J | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2879 | |

DATE MAILED: 10/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/722,705 | YANAGISAWA, YOSHIHIRO | |
| | Examiner | Art Unit | |
| | Kenneth J. Ramsey | 2879 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6-8,10-12,14 and 17-19* is/are allowed.

6)☒ Claim(s) *1,2,5,9,13,15,16 and 20-23* is/are rejected.

7)☒ Claim(s) *3 and 4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Request for Continued Examination*

Acknowledgement is made of applicants request for continue examination. New claims 20-23 have been added and an argument made with respect to the rejected claims.

### *Non Prior Art Rejections*

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 20-23 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the description and enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. These claims recite a process of manufacture of the surface conduction field emission source including the connection of both a scanning circuit and a modulating circuit to the column wirings of the emission source. Applicants have not disclosed an operable field emission source having the scanning circuit connected to the same electrodes as the modulating circuit. Instead applicant discloses the connection of the modulating circuit to one of the row and column wire sets and connection of the scanning circuit to the other of the row and column wire sets.

***Prior Art Rejections***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 5, 13, 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Banno et al, patent 6,060,113, (Banno) in view of Tokai et al, patent 6,312,864 (Tokai). Banno discloses a process of forming a surface conduction emissive device comprising forming electrode pairs on a substrate, forming row wires connected to first electrodes of each pair and forming column wires connected to a second electrodes of each pair. Also, Banno discloses forming an emissive film by an inkjet process and "forming" the film by passing current through the film to create fissures, which provide an electron emissive source. Further Banno, column 42, lines 55-64, discloses that a photolithographic process may form the row and column wires. The particular photolithographic process is not taught, but it is clear that the row-directional wires are separated from the column directional wires by an insulator at each intersection in the process. Thus Banno suggests a multiple step process of first forming the row or the column wires, then the insulator, then the other of the column or row wires, wherein each of the steps of forming the wires corresponds to a commonplace photolithographic step of depositing a high definition wire. Such a high definition process is known from Tokai et al, column 2, line 66 through column19-35, wherein feeder wires in a display device are be formed by depositing a photosensitive

[redacted]

film comprising conductive metal particles, exposing and developing the film, then baking. It would also have been obvious that, if sinterable insulator particles were substituted for conductive particles, a pattern of insulators would be similarly formed. It thus would have been obvious to one of ordinary skill in the art at the time of applicant's invention to form the wire and column wires of Banno, by the photolithographic process of Tokai since Banno suggests the use of a photolithographic process where a high definition wiring matrix is required. Now the order of the photographic steps will be discussed. Where the spacing of the row wires differs from the spacing of the column wires, the order of steps obviously should proceed with the wires which have a closer spacing than the other since a substrate which is more planar (without any prior forming of wires or spacers) provides for better resolution in the photographic process. While applicant states that Banno does not disclose that the column wires have a smaller spacing than that of the row wires, the examiner respectfully notes that the spacing of rows and columns should follow that of the pixel patterns, figures 8A and 8B. In each figure, it can be seen that the pixels have a greater row spacing than a column spacing. Only one row is shown in figure 8A whereas 6 columns are shown. In figure 8B, five rows of pixels are shown whereas seven columns of pixels are shown. Thus the column wires must be more closely spaced than the row wirings because the row and column wires are spaced so as to address the pixels. It follows that (1) the column wires must be spaced more closely than the row wires and (2) that one of ordinary skill in the art would have formed the column wires first since the planar substrate allows for a better resolution when the higher resolution column wire array is formed.

[redacted]

3. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Banno and Tokai as applied to claim 1 above, and further in view of Mitsutake et al 5,760,538 (Mitsutake '538). Mitsutake '538 is cited to support the Official notice in the prior Office action re use of spacers located on the row electrodes. See Figure 2 for this teaching. Since the flat panel display form by Banno has a similar atmospheric loading the use of spacers on the row electrodes as taught by Mitsutake '538 to support the load therein would have been obvious.

4. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Banno and Tokai as applied to claim 1 above, and further in view of Mitsutake et al, patent 5,594,296 (Mitsutake '296). Claim 15 combines the sep of forming the column wires by a photolithographic step with a step of forming the row wires by a screen printing step. Since the row wires of Banno require a lower resolution than the column wires and since the same combination of steps was employed in Mitsutake '296, column 13, line 51 through column 46, to respectively form the column and row wires, such a process would have been obvious in Banno in order to obtain a relatively high definition display at the lowest possible cost.

5. Claims 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Banno and Tokai as applied to claim 1 above, and further in view of Suzuki et al 5,593,335 (Suzuki). These claims are construed for purposes of this rejection to add to the recitations of claim 1 the features of connecting a modulating circuit and a scanning circuit respectively to the one of the row and column wire sets and to the other of the row and column wire sets. Such a feature is well known in the art as shown by Suzuki

column 16, lines 19-46, and would have been obvious to one of ordinary skill in the art in order to obtain a high resolution display including a video display.

6. Claims 3 and 4 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claims 6-8, 10-12, 14 and 17-19 are allowed.

8. The following is a statement of reasons for the indication of allowable subject matter: claims 3, 10-12 and 14 are drawn to allowable subject matter since the prior art does not teach or suggest providing row and column conductors of a field emissive display by depositing a photosensitive film through a plurality of apertures of a mask on to a substrate, selectively exposing the film deposits to form row and column electrodes. Claim 4 is allowable since although it was known to deposit the pair of electrodes by offset printing, it was not taught or suggested to combine the offset printing process with the other steps of this claim such as forming the column wires by a photolithographic step. For instance Yanagisawa et al, patent 5,996,488, taught the use of offset printing to form large area displays not suitable to photolithographic steps, but the resolution of the display was at such a level that both the column wires and row wires were formed by the cheaper screen printing process. Claims 6 through 8 and 17-19 are allowable since the prior art does not teach or suggest forming the row wires with a different cross section than the column wires.

9. Applicant's arguments filed June 27, 2003 have been fully considered but they are not persuasive. As noted above, the argument that Banno does not teach or

suggest the smaller spacing of the column wires to one of ordinary skill in the art is erroneous. The spacing of the column and row wires is suggested by the type of display. Since displays with different pixel spacing in the x and y directions are well known as shown by Banno, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to have a corresponding spacing of the column and row wires since the column and row wires are arranged to address the pixels. As to the fact that Tokai does not form a matrix of wires having crossovers by a photographic step, the rejection is based upon a combination of Banno with Tokai. Banno teaches the forming of a matrix of wires having crossovers that are insulated and that either the row or column wires or both could be form photographically. Thus one of ordinary skill in the art would have recognized that the process of Tokai could be applied to the row and column wires of Banno to obtain a higher resolution.

Directions for Responses

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth J. Ramsey whose telephone number is 308-2324. The examiner can normally be reached on Monday-Friday from 9:00 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimesh Patel, can be reached on (703) 305-4794. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 308-0956.

Kenneth J. Ramsey

KENNETH J. RAMSEY
PRIMARY EXAMINER